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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 12

Application Number: 09/283,231
Filing Date: April 01, 1999
Appellant(s): KUROSE, YOSHIKAZU

Ronald P. Kananen
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 5/28/2002.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

Appellant's brief includes a statement that claims 1-3, 5-8, 10, 22-24, and 26-29 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

Appellant's brief includes a statement that claims 4, 9, 25 and 30 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

Appellant's brief includes a statement that claims 11, 13, 15, 19, 31, 33, and 38 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

Appellant's brief includes a statement that claims 12 and 32 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

Appellant's brief includes a statement that claims 16 and 35 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

Appellant's brief includes a statement that claims 17 and 36 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

Appellant's brief includes a statement that claims 18 and 37 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

Appellant's brief includes a statement that claims 21 and 40 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

Appellant's brief includes a statement that claims 14, 20, 34, and 39 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,179,638	Dawson et al	01-1993
5,977,987	Duluk, Jr. etal	11-1999
5,742,796	Huxley	04-1998
JP 09130570	Kiyoto	05-1997

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-40 rejected under 35 U.S.C. 103. This rejection is set forth in prior Office Action, Paper No. 9, and is repeated here for reference.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 5-8, 10, 22-24, and 26-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dawson (US Patent 5,179,638), in view of Kiyoto (09130570: Patent Abstracts of Japan: Publication Date 16-05-97).

Claim 27, claims a method of expressing an image as a composite of graphic units of predetermined shape, comprising the steps of judging whether or not a pixel is positioned within a unit graphic for each of the pixels among a plurality of pixels being simultaneously processed in parallel in plurality of pixel processing circuits, stopping the operation of pixel processing for pixels not within the graphic units based on the outcome of the judging step.

As per claim 27, Dawson teaches distributed processing using parallel pipelines (processing a plurality of pixels in a plurality of pixel processing circuits), and then recombining the parallel pixel flow into a single memory module known as a frame buffer (Col.2: lines 46-50; Col.11: lines 51-62). Dawson also teaches interpolating values for the interior points (Col.6: lines 65-66), thus teaching implicitly, a judging means that determined these pixels to be interior

pixels. Dawson, while not teaching setting a valid bit flag for this condition, does teach setting a polygon "end" bit in the last vertex of the polygon, and checking that flag while rendering the primitive (setting a bit to flag a condition). Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to set a valid bit when the pixels were judged to be inside the polygon, and check the flag during pixel value computations, in order to reduce computational overhead. Dawson however fails to teach stopping the operation of the pixel processing circuits for pixels that do not lie within the unit graphics. Kiyoto teaches a method to prevent useless power consumption by stopping the application of an image clock signal to a processing block not in use (Abstract). Hence it would have been obvious to one of ordinary skill in the art at the time the invention was made, to use Kiyoto's teaching to stop the operation of the pixel processing circuits for pixels that do not lie within the unit graphics in the invention of Dawson, in order to prevent useless power consumption.

Claim 22 is similar to claim 27, and hence is rejected with the same rationale.

Claim 28 adds to claim 27, the steps of supplying clock signal to pixel processing circuits for pixels within the graphic unit, and stopping the supply of clock signal to circuits for pixels that do not lie inside the graphic unit.

As per claim 28, Kiyoto teaches a supply/inhibit signal generating section, generating a signal to inhibit the application of the image clock signal to a processing block not relating to the image processing (Abstract).

Claim 23 is similar to claim 28, and hence is rejected with the same rationale.

Claim 29 adds to claim 28, the step of each of the pixel processing circuits performing pipeline processing by a plurality of processing circuits connected in series.

As per claim 29, Dawson teaches a plurality of processing circuits connected in series, for example, symbol generator, geometry engine, tiling engine, etc. (Fig.5).

Claim 24 is similar to claim 29, and hence is rejected with the same rationale.

Claim 26 adds to claim 22, the step of processing the R, G, B output values of a pixel.

As per claim 26, Dawson teaches that the R, G, B values are independently calculated when rendering polygons (Col.8: lines 55-58).

Claims 1-3 and 5-8 are claims to apparatus that perform the methods of claims 22-24 and 26-29 respectively, and hence, are rejected with the same rationale.

Claim 10 adds to claim 6 the steps of the pixel position judging circuit adding validity data to of the result of the judgement to pixel data, and the control circuit judging whether to stop the operation of the pixel processing circuits based on the validity data.

As per claim 10, Dawson teaches interpolating values for the interior points (Col.6: lines 65-66), thus teaching implicitly a judging means that determined these pixels to be interior pixels. Dawson does not teach setting a valid bit flag for this condition. However, Dawson

teaches setting a polygon "end" bit in the last vertex of the polygon, and checking that flag while rendering the primitive. Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to set a valid flag when the pixels tested were judged to be inside the polygon, and check the flag during pixel value computations, so that wastage of resources, in determining values for pixels that will not be displayed, may be avoided.

Claims 4, 9, 25, and, 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dawson (US Patent 5,179,638), in view of Kiyoto (09130570: Patent Abstracts of Japan: Publication Date 16-05-97), as applied to claim 27, and further in view of Duluk, Jr. (US Patent 5,977,987).

Claim 30 adds to claim 29, the step of the pixel processing circuit having a flag storage portion, connected in series to constitute a shift register, and the shift register being used to control the pipeline processing and supply of clock signal.

As per claim 30, Duluk teaches a rendering system wherein a flag memory storage means is used to store a flag bit equal to the query result, and a shifting means for conditionally shifting data stored in data fields, wherein the shifting means includes a shift register bit connected to the storage bits of storage means (Claims 29 and 34). Hence it would have been obvious to one of ordinary skill in the art at the time the invention was made, to connect the flag storage portion to the shift register in series as taught be Duluk, in the invention of Dawson, to control the pipeline processing, since use of registers in processing was known to be much faster than access to other memory locations, since the registers resided in the CPU.

Claim 25 is similar to claim 30 and hence is rejected with the same rationale.

Claims 4 and 9 are claims to apparatus that perform the methods of claims 25 and 30 respectively, and hence, are rejected with the same rationale.

Claims 11-13, 15, 16-19, 21, 31-33, 35-38, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dawson (US Patent 5,179,638), in view of Huxley (US Patent 5,742,796), and Kiyoto (09130570: Patent Abstracts of Japan: Publication Date 16-05-97).

Claim 31 claims a image processing method comprising the steps of using a plurality of pixel processing circuits to simultaneously blend a plurality of first pixel data and a plurality of second pixel data indicated by a blending ratio data set for each pixel, judging based on the blending ratio data whether to perform said blending by pixel processing circuits, and stopping the operation of the corresponding pixel circuits when judging that they will not perform said blending.

As per claim 31, Dawson teaches distributed processing using parallel pipelines (processing a plurality of pixels in a plurality of pixel processing circuits), and then recombining the parallel pixel flow into a single memory module known as a frame buffer (Col.2: lines 46-50; Col.11: lines 51-62). Dawson however fails to teach the use of blending ratio data in pixel processing. Huxley teaches an alpha blend unit (Col.61), which blends the source color and destination color in the given ratios, to produce an output color, as shown by the equation

(Col.61: line 16). Huxley also teaches a NoAlphaBuffer bit in the AlphaBlendMode message that controls alpha blending, wherein the setting of the NoAlphaBuffer bit or the absence of an alpha value causes the alpha blending to be bypassed. Hence it would have been obvious to one of ordinary skill in the art at the time the invention was made, to include the blending ratio pixel processing of Huxley in the texture engine of Dawson, in order to provide more realistic results. Dawson and Huxley, however fails to teach stopping the operation of the pixel processing circuits for pixels that do not lie within the unit graphics. Kiyoto teaches a method to prevent useless power consumption by stopping the application of an image clock signal to a processing block not in use (Abstract). Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to use Kiyoto's teaching to stop the operation of the pixel processing circuits for pixels that do not lie within the unit graphics or do not need alpha blending, in the invention of Dawson and Huxley, in order to prevent useless power consumption.

Claims 32-33 are similar to claims 28 and 29 respectively, and hence are rejected with the same rationale.

Claim 35 claims a method of expressing an image as a composite of graphic units of predetermined shape, comprising the steps of using a plurality of pixel processing circuits to blend a plurality of first pixel data and a plurality of second pixel data indicated by a blending ratio data set for each pixel, judging whether or not a pixel is positioned within a unit graphic for each of the pixels among a plurality of pixels being simultaneously processed in parallel in

plurality of pixel processing circuits, stopping the operation of pixel processing for pixels not within the graphic units based on the outcome of the judging step.

As per claim 35, Dawson teaches distributed processing using parallel pipelines (processing a plurality of pixels in a plurality of pixel processing circuits), and then recombining the parallel pixel flow into a single memory module known as a frame buffer (Col.2: lines 46-50; Col.11: lines 51-62). Dawson also teaches interpolating values for the interior points (Col.6: lines 65-66), thus teaching implicitly, a judging means that determined these pixels to be interior pixels. Dawson fails to teach blending of pixel data. Huxley teaches an alpha blend unit (Col.61), which blends the source color (first pixel data) and destination color (second pixel data) in the given ratios, to produce an output color (third pixel data), as shown by the equation (Col.61: line 16). Huxley also teaches a NoAlphaBuffer bit in the AlphaBlendMode message that controls alpha blending, wherein the setting of the NoAlphaBuffer bit or the absence of an alpha value causes the alpha blending to be bypassed. Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to combine the blending ratio pixel processing of Huxley with the interpolation processing of Dawson, to interpolate the color texture values for the interior pixels, for greater efficiency in pixel processing. Dawson and Huxley, however fails to teach stopping the operation of the pixel processing circuits for pixels that do not lie within the unit graphics. Kiyoto teaches a method to prevent useless power consumption by stopping the application of an image clock signal to a processing block not in use (Abstract). Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to use Kiyoto's teaching to stop the operation of the pixel processing

circuits for pixels that do not lie within the unit graphics or do not need alpha blending, in the invention of Dawson and Huxley, in order to prevent useless power consumption.

Claim 36 claims a image processing method comprising the steps of using a plurality of pixel processing circuits to process simultaneously, to produce a plurality of second pixel data from a plurality of first pixel data, comparing depths of plurality of first pixel with the depths of plurality of third pixels stored in a storage unit, judging whether or not to rewrite the third pixel data by the second pixel data, and stopping the operation of the corresponding pixel circuits when judging that they will not perform said rewrite.

As per claim 36, Dawson teaches distributed processing using parallel pipelines (processing a plurality of pixels in a plurality of pixel processing circuits), and then recombining the parallel pixel flow into a single memory module known as a frame buffer (Col.2: lines 46-50; Col.11: lines 51-62), thus also teaching producing plurality of second pixel data from a plurality of first pixel data. Dawson however does not teach depth comparison between pixel data. Huxley also teaches a depth test, which compares a new fragment's depth (second depth data of third pixel data), against the corresponding depth in the depth buffer (first depth data of first pixel data), and updating the frame buffer if the test passed, and ignoring the new fragment depth data if the test failed (Col.7: lines 8-33, Col.10: lines 8-60, Col.31: lines 12-20, Col.51: lines 25-65). Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to use the depth test as taught by Huxley, in the texture engine of Dawson, in order to be able to render the images in the correct perspective, taking into account the

occluding properties of the objects rendered. Dawson and Huxley, however fails to teach stopping the operation of the pixel processing circuits for pixels that do not lie within the unit graphics. Kiyoto teaches a method to prevent useless power consumption by stopping the application of an image clock signal to a processing block not in use (Abstract). Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to use Kiyoto's teaching to stop the operation of the pixel processing circuits for pixels that do not lie within the unit graphics or do not need alpha blending, in the invention of Dawson and Huxley, in order to prevent useless power consumption.

Claims 37 and 38 are similar to claims 28 and 29 respectively, and hence are rejected with the same rationale.

Claim 40 claims a image processing method comprising the steps of using a plurality of pixel processing circuits to process simultaneously, to produce a plurality of second pixel data from a plurality of first pixel data, comparing depths of plurality of first pixel with the depths of plurality of third pixels stored in a storage unit, judging whether or not to rewrite the third pixel data by the second pixel data, and judging whether or not a pixel is positioned within a unit graphic for each of the pixels among a plurality of pixels being simultaneously processed in parallel in plurality of pixel processing circuits, and stopping the operation of the corresponding pixel circuits when judging that they will not perform said rewrite, or the pixel is not positioned within the unit graphic.

Claim 40 is a combination of claims 35 and 36, and hence is rejected with the same rationale as claims 35 and 36.

Claims 11-13 are claims to apparatus that perform the methods of claims 31 and 33 respectively, and hence, are rejected with the same rationale.

Claim 15 adds to claim 11 the steps of providing a storage circuit for storing second pixel data, and the control circuit rewriting the second pixel data by the first pixel data when blending will not be performed, and rewriting by the third pixel data when blending will be performed.

As per claim 15, Huxley teaches an alpha blend unit (Col.61), which blends the source color (first pixel data) and destination color (second pixel data) in the given ratios, to produce an output color (third pixel data), as shown by the equation (Col.61: line 16). Huxley also teaches a NoAlphaBuffer bit in the AlphaBlendMode message that controls alpha blending, wherein the setting of the NoAlphaBuffer bit or the absence of an alpha value causes the alpha blending to be bypassed, and when the alpha blending is disabled, the color is passed on unchanged. It is obvious from the equation $C_o = C_sS + C_dD$, that when there is no blending, the source color is the output color, implying that the second pixel data is replaced by the first pixel data when blending will not be performed, and, the output color (third pixel data) is written to the destination buffer (second pixel data), otherwise. Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to include the alpha blending unit in the texture engine of Dawson, in order to render objects in proper perspective.

Claims 16-19 are claims to apparatus that perform the methods of claims 35-38 respectively, and hence, are rejected with the same rationale.

Claim 21 is a claim to an apparatus that performs the method of claim 40, and hence, is rejected with the same rationale.

Claims 14, 20, 34, and, 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dawson (US Patent 5,179,638), in view of Huxley (US Patent 5,742,796), and Kiyoto (09130570: Patent Abstracts of Japan: Publication Date 16-05-97), as applied to claims 11, 17, 31, and 36 respectively, and further in view of Duluk, Jr. (US Patent 5,977,987).

As per claims 14, 20, 34, and 39, Duluk teaches a rendering system wherein a flag memory storage means is used to store a flag bit equal to the query result, and a shifting means for conditionally shifting data stored in data fields, wherein the shifting means includes a shift register bit connected to the storage bits of storage means (Claims 29 and 34). Hence it would have been obvious to one of ordinary skill in the art at the time the invention was made, to connect the flag storage portion to the shift register in series as taught be Duluk, in the invention of Dawson, to control the pipeline processing, since use of registers in processing was known to be much faster than access to other memory locations, since the registers resided in the CPU.

(11) Response to Argument

In response to appellant's argument that

- an image clock signal is inhibited for an entire processing block, not just for selected pixels or pixel processing circuits within a processing block, it is noted that Kiyoto teaches inhibiting clock signals to processing blocks that do not receive image data. Therefore, the processing blocks are devices, some of which are inhibited by image clock signal, and stopped from performing wasteful processing, when these devices do not receive image data (these devices did not receive valid data). Similarly, in the current application, the parallel pixel processing circuits are devices that perform calculations on pixels. Dawson teaches interpolating values for the interior pixels of a polygon for rendering. It is inherent in Dawson that the pixels lying outside the polygon not be processed, since they would not be rendered. Therefore Kiyoto is mainly cited to teach the step of inhibiting power supply to at least one of the pixel processing circuits (devices) that did not receive valid data.
- Kiyoto does not teach a device for use with "polygon rendering", it is noted that Kiyoto does deal with image processing devices, and image processing means wherein pixel data is generated from image data input.
- There is no teaching/suggestion in Kiyoto of stopping an image clock signal to selected pixel processing circuits to be processed simultaneously, it is noted that Kiyoto's processing blocks are devices similar to the processing circuits of the invention, and the power supply is inhibited via image clock signals to some of these devices. Hence, this teaching could be applied to the processing circuit devices of the current invention.

- There is no teaching/suggestion in Kiyoto of stopping an image clock signal to selected pixel processing circuits based on a judgement that the corresponding pixel is positioned outside a graphic unit to be processed, and the claimed "control circuit for stopping at least one of said pixel processing circuits .....", and the claimed "control circuit for stopping at least one of said pixel processing circuits ... based on the judgement of the position judging circuit", it is noted that Dawson is relied on to teach a judgement that the corresponding pixel is positioned outside a graphic unit (Col.6: lines 65-66: interpolate the interior points, teaching implicitly the judgement of whether a given pixel is interior or exterior).
- Huxley does not teach a judging step that controls whether or not the pixel processing circuits will perform blending, it is noted that Huxley teaches the use of NoAlphabuffer bit in the AlphaBlendMode message that is received by the pixel processing circuits, thus teaching a judging means that determines whether Alpha blending will be performed based on the presence/absence of alpha values for the pixel, and Kiyoto makes it obvious to stop the pixel processing circuits that do not have data to be processed. As per the argument that Huxley does not teach a system or method in which a determination is made whether alpha blending will be performed, it is noted that no blending would be performed when NoAlphabuffer is set, and AlphaBlendMode provides for alpha blending, thus providing the method to determine if alpha blending would be performed.

- As per the argument regarding claims 12 and 32 that Huxley teaches away from stopping a pixel processing circuit for alpha blending by stating that the messages should continue to be passed to other units, it is noted that the pixel processing circuits would still need to process other attributes associated with the pixel in subsequent clock cycles, and hence, Huxley is not seen to teach away from what is claimed.
- The Examiner's statement that "Huxley would still need to process other attributes associated with the pixel in subsequent clock cycles" is inconsistent with the language of claim 12, it is noted that the respective pixels would not be updated for alpha values, and hence the pixel processing circuits would be stopped for the clock cycles that are used for alpha blending. But, no alpha blending does not imply that these pixels would not be rendered. Hence, in the event that these pixels would be rendered, it is possible for these pixels to undergo other processing by other units, before being written to the frame buffer. Hence, the examiner's statement is not inconsistent with the language of claims 12 and 32. This explanation also applies to claims 17 and 36.
- Teaching of Kiyoto are directed to color copiers, scanners, and the like, and have little reference to 3D image processing technology, it is noted that Kiyoto teaches inhibiting signals to an image processor, thus reducing power consumption. This teaching could be used to inhibit signals to pixel processing circuits, thus reducing power consumption.

- Regarding claims 18 and 37, Huxley does not teach or suggest a system in which a clock signal is stopped to stop the operation of a pixel processing circuit after determining that it will not perform a rewrite of depth data in a storage circuit, it is noted that determining whether to perform a rewrite of a depth data has not been claimed.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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July 11, 2002

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